

What is claimed is:

10035175.010402

1 1. A method of forming a shallow trench isolation,
2 comprising steps of:
3 forming a plurality of trenches in a semiconductor
4 substrate;
5 forming an oxide liner on the bottom and sidewall of each
6 trench; and
7 thermal annealing in a nitrogen-containing atmosphere to
8 dope nitrogen elements in the oxide liner, wherein a
9 nitrogen-rich layer is formed at the interface between the
10 oxide liner and the semiconductor substrate.

1 2. The method according to claim 1, wherein the
2 nitrogen-containing atmosphere comprises N_2 , NH_3 , N_2O , nitric
3 oxide or any nitrogen-containing compound.

1 3. The method according to claim 1, wherein the thermal
2 annealing is performed at 650~850°C, 100~250 mtorr, for 1~30
3 minutes.

1 4. The method according to claim 1, wherein the oxide liner
2 is formed by thermal oxidation.

1 5. The method according to claim 1, wherein the trenches
2 are formed by anisotropical dry etch.

1 6. The method according to claim 1, further comprising
2 steps of:

3 depositing an insulating layer on the entire surface of

- 4 the semiconductor substrate to fill the trenches; and
5 using chemical mechanical polishing (CMP) to planarize
6 the insulating layer to reach the top of the semiconductor
7 substrate.